REMARKS

Claims 2, 8, and 10 are amended hereby. Claims 22-23 are canceled. Claim 25 is added. Accordingly, after entry of this Amendment, claims 2, 5-6, 8, 10, and 24-25 will remain pending.

In the non-final Office Action dated November 30, 2005, the Examiner rejected claims 2, 5, 6, 8, 10, and 22-24 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the Applicant regards as the invention. In particular, the Examiner stated, with respect to claims 2 and 10, that the phrase "that portion of said semiconductor substrate" is unclear. For claim 8, the Examiner stated that the phrase "an upper surface of said interlayer insulating film being substantially equal to an upper surface of said gate electrode" is vague and indefinite. For claim 22, the Examiner stated that the phrase "the lower end of the gate electrode is cut out" is unclear as to what is meant. Turning to claim 23, the Examiner stated that the phrase "the second gate insulating film" is unclear. While the Applicant respectfully disagrees with these rejections, the Applicant has amended (or canceled) the claims and believes that the amendments (or cancellations) address the Examiner's rejections. Accordingly, the Applicant respectfully requests that the Examiner withdraw the rejections under 35 U.S.C. § 112.

Next, the Examiner objected to claim 8, finding that the phrase "said gate side wall insulating film" has no antecedent basis. With respect to claim 10, the Examiner objected, stating that the phrase "the conductivity type of said semiconductor substrate" has no antecedent basis. The Applicant respectfully apologizes for these typographical oversights. In response, the Applicant presents amendments that are believed to address the Examiner's objections. As a result, the Applicant respectfully requests that the Examiner withdraw the objections to claims 8 and 10.

Finally, in the Office Action, the Examiner objected to claim 10, finding that it would be allowable if rewritten to overcome the rejections under 35 U.S.C. § 112, second paragraph. The Applicant would like to thank the Examiner for this indication of allowable subject matter. In view of the amendments made to claim 10, the Applicant respectfully submits that the rejections and objections with respect to claim

10 have been addressed. Accordingly, the Applicant respectfully submits that claim 10 is now in a condition for allowance.

Claims 2, 5, 6, 8, 22, and 24 were rejected under 35 U.S.C. § 103(a) as unpatentable over Maruo (U.S. Patent No. 5,181,090) in view of Shell et al. (U.S. Patent No. 5,429,956). The Applicant respectfully disagrees with this rejection and, therefore, respectfully traverses the same.

Claims 2, 5-6, 8, and 24-25 are patentably distinguishable over the references cited by the Examiner because the claims recite a semiconductor device that combines a number of elements including, for example, a gate electrode having a first gate portion formed on the first insulating film portion and a second gate portion formed on the second insulating film portion, in which the first and second gate portions are formed of the same material, an edge portion of the gate electrode side of the first diffusion layers being located outside of a side surface of the gate electrode. Since neither of the cited references describe or suggest such a combination, the Applicant respectfully submits that the claims are patentable over the cited references.

Maruo describes a high voltage CMOS device where the edge portion of the gate electrode 16 overlaps the sides of the first diffusion layers 17, 18a. (Maruo at Fig. 1, for example.) In other words, the sides of the first diffusion layers 17, 18a are located beneath the gate electrode 16, interiorly of the side surfaces of the gate electrode 16. (Maruo at Fig. 1, for example.) As understood by the Applicant, the construction of the CMOS device described by Maruo results from ion implantation (of boron) in the n-well region 13 to form the p- offset regions 17. (Maruo at col. 7, line 63, through col. 8, line 6.) Ion implantation into the n-well region 13 occurs where there are no silicon nitride sections 26. (Maruo at Fig. 3(c), for example.) The gate electrodes 16 extend between and overlap with adjacent p- offset regions 17. (Maruo at Fig. 3(f), for example; see also col. 8, lines 38-47.)

Shell et al. does not cure the deficiencies noted with respect to Maruo et al. Specifically, Shell et al. describes a method for fabricating a field effect transistor. The structure of the completed transistor is illustrated, for example, in Fig. 9. The Applicant respectfully directs the Examiner's attention to the edge portions of the gate electrode 22. As illustrated, the side edges of the gate electrode 22 are flush with the

edges of the first diffusion layers 60, 62. More specifically, the edges of the first diffusion layers 60, 62 are not located outside of the side surface of the gate electrode 22. (Shell et al. at Fig. 9, for example.) The Applicant respectfully directs the Examiner's attention to col. 6, lines 39-52, of Shell et al. As this passage makes clear, after removal of the silicon oxide layer 26 and sidewall spacers 30 (see Fig. 8), the source/drain region 60 is formed by implanting N-type dopant species in the P-substrate. (Id.) Since the sidewall spacers 50 are formed after the doping of the P-substrate, the Applicant respectfully submits that the edges of the source/drain region 60 must at least be flush with the edges of the gate electrode 22. As a result, there is nothing in Shell et al. that may be said to describe or suggest a construction that includes, among other features, a gate electrode having a first gate portion formed on the first insulating film portion and a second gate portion formed on the second insulating film portion, in which the first and second gate portions are formed of the same material, an edge portion of the gate electrode side of the first diffusion layers being located outside of a side surface of the gate electrode. Accordingly, the Applicant respectfully submits that Shell et al. cannot be combined properly with Maruo to render obvious any of claims 2, 5-6, 8, and 24-25.

All matters having been addressed and in view of the foregoing, Applicants respectfully request the entry of this Amendment, the Examiner's reconsideration of this application, and the immediate allowance of all pending claims.

Applicants' Counsel remains ready to assist the Examiner in any way to facilitate and expedite the prosecution of this matter. Please charge any fees associated with the submission of this paper to Deposit Account Number **033975**, Order No. **008312-0304355**.

The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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